FPGA Implementation of Power Converters for High-Speed PHILS Interface

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Introduction

- **Power Hardware-In-the-Loop Simulation (PHILS)**
  - Real-time hardware-based simulation for complex systems
  - Essential for microgrids system analysis and design
  - Needs high-performance real-time digital computer

- **KIER PHILS Test Beds**
  - Real-time computer : RTDS
  - Simulation and test for renewable microgrids system and component
  - Needs many power electronic converters and their interface
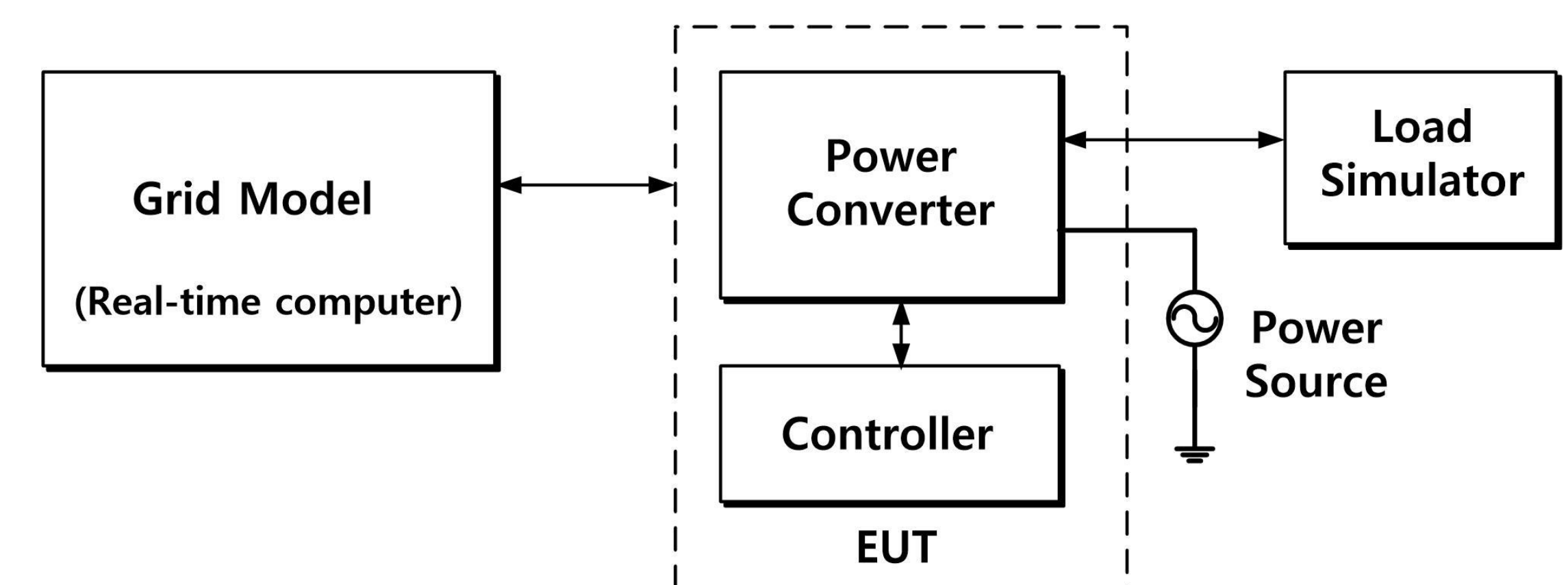
- **Problems of Power Electronics Interface in PHILS**
  - Power converter is a fast dynamic system (~ few kHz bandwidth)
  - Latency problem (> 50us (20kHz) in RTDS) : computational burden
  - Difficult to interface PWM control signals
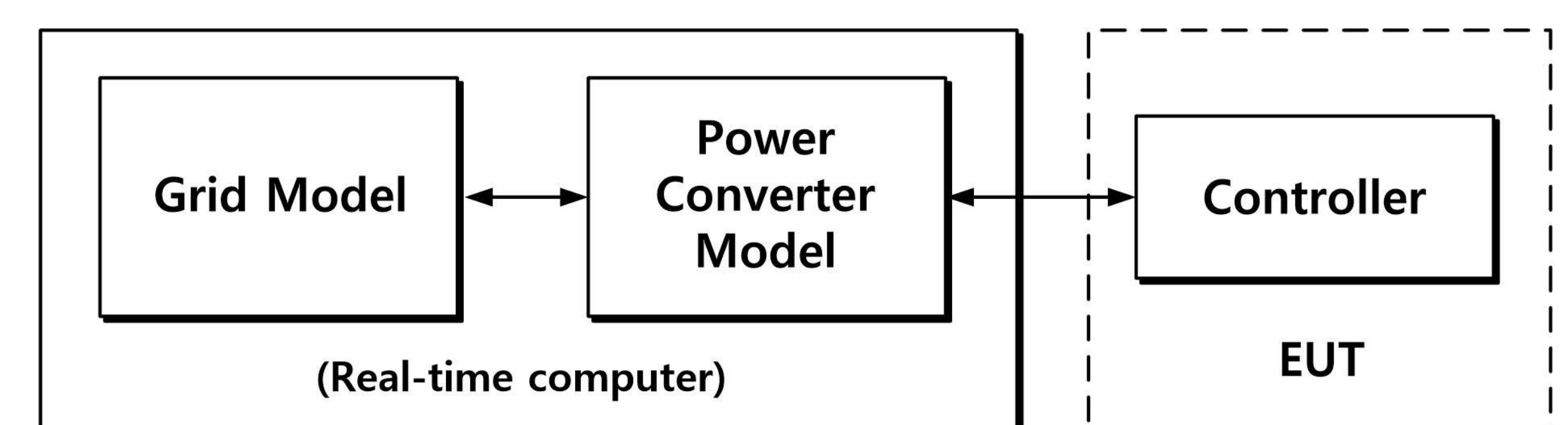
- **Possible Solution**
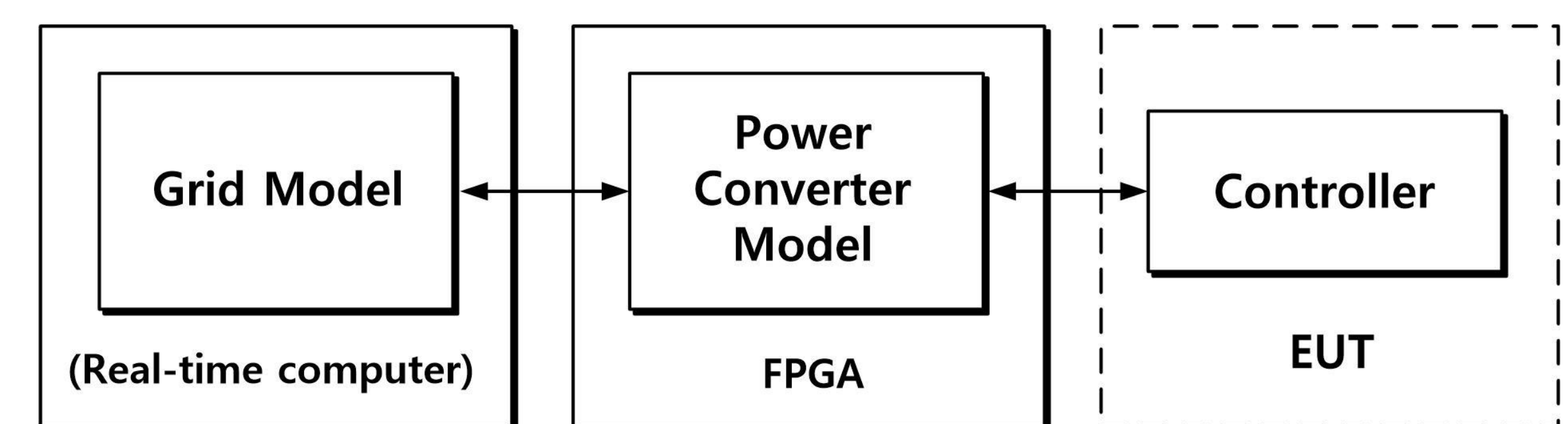 - FPGA-based co-processing for power electronics converters

Methods of HILS Test

- **Full Converter Hardware Test with Load Simulator**

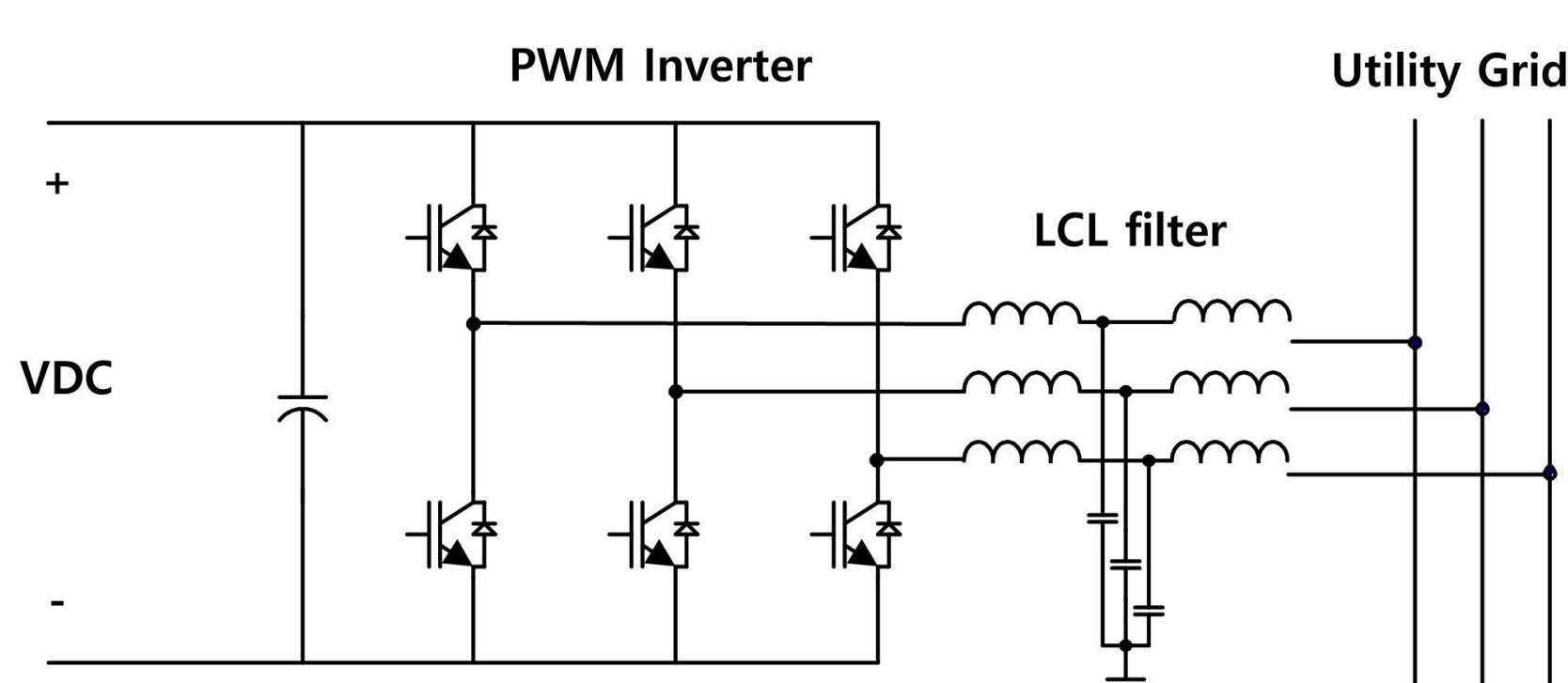- **Controller Test (Converter embedded in RTDS)**

- **FPGA-based Controller Test (Proposed)**
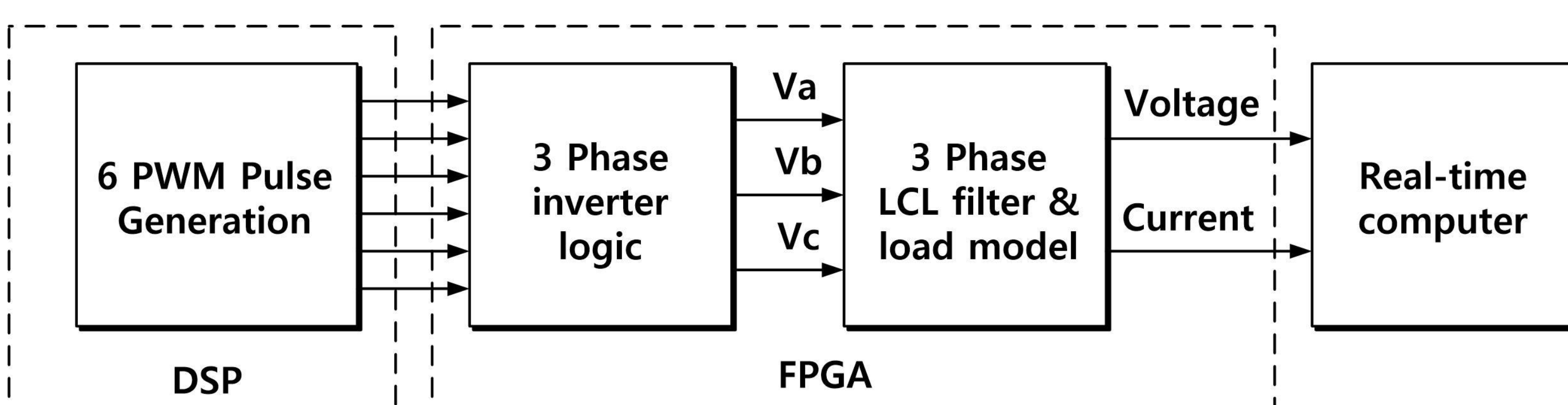
FPGA Design

- **Target Power Converter**
  - 3 phase PWM inverter

- **Design Procedure**

Continuous-time modeling → Discretization → VHDL Programming & verification

- **Structure**

DSP: 6 PWM Pulse Generation → FPGA: 3 Phase inverter logic (Va, Vb, Vc) → 3 Phase LCL filter & load model (Voltage, Current) → Real-time computer
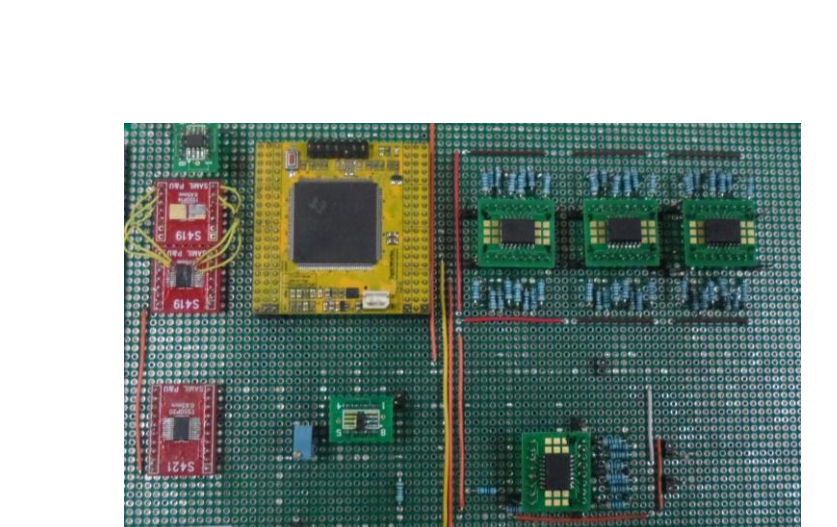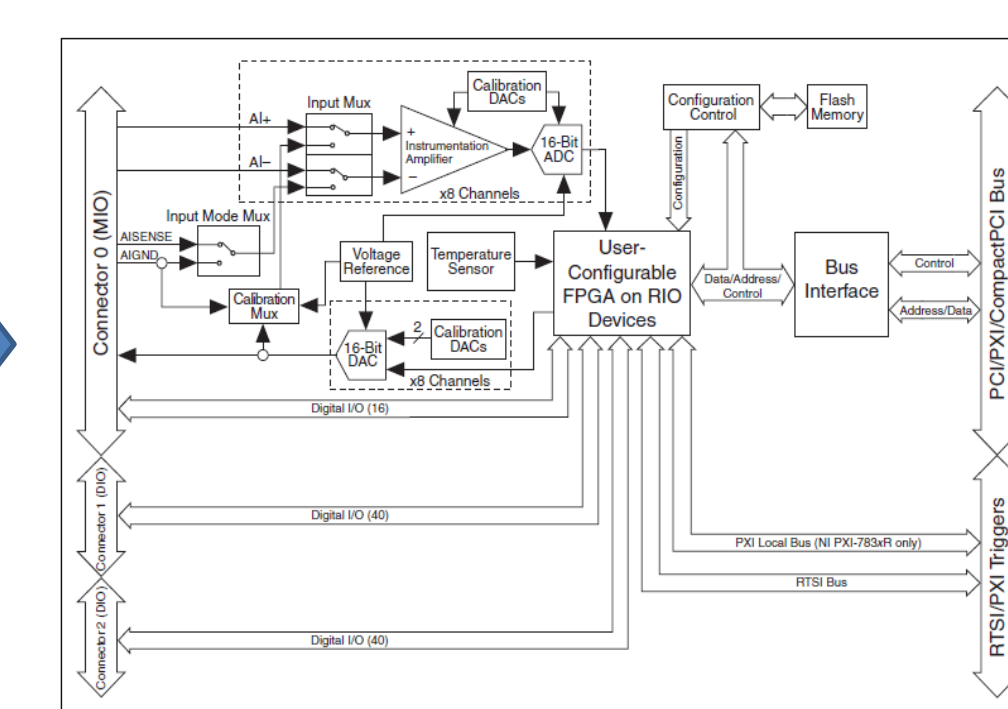
Implementation

- **FPGA Implementation**

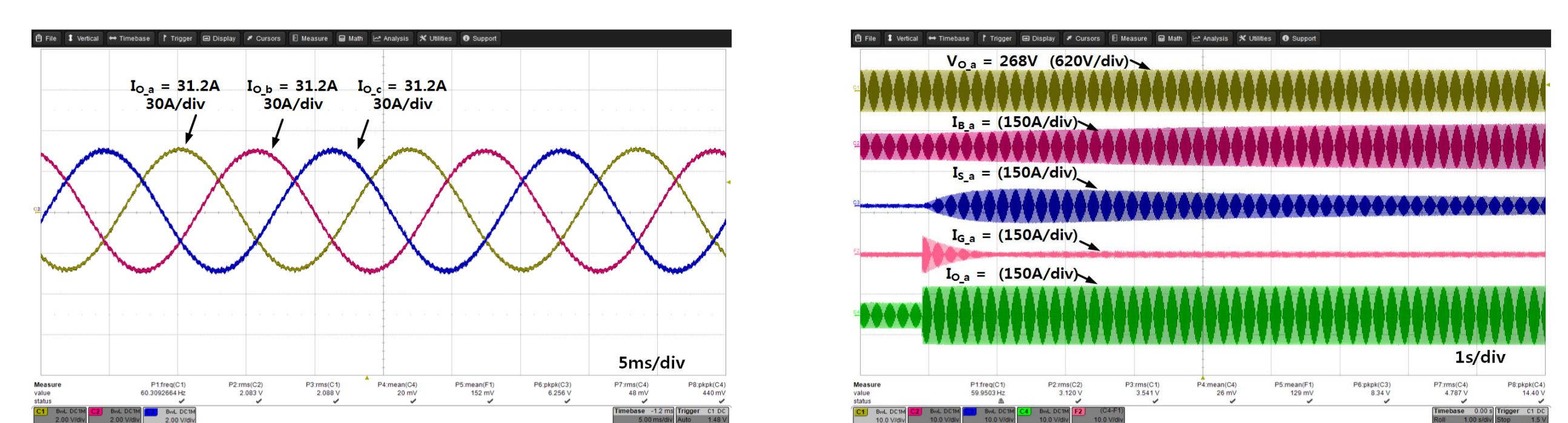DSP TMS320F28335   Xilinx Virtex-5 LX30   RTDS

- **Test Results**

Inverter waveforms on RTDS

- **Conclusions**
  - FPGA-based design and implementation of power converter for low latency PHILS interface
  - Modeling and implementation using VHDL on Virtex-5 LX30
  - Test and verification with RTDS